

FIG. 1

1/29

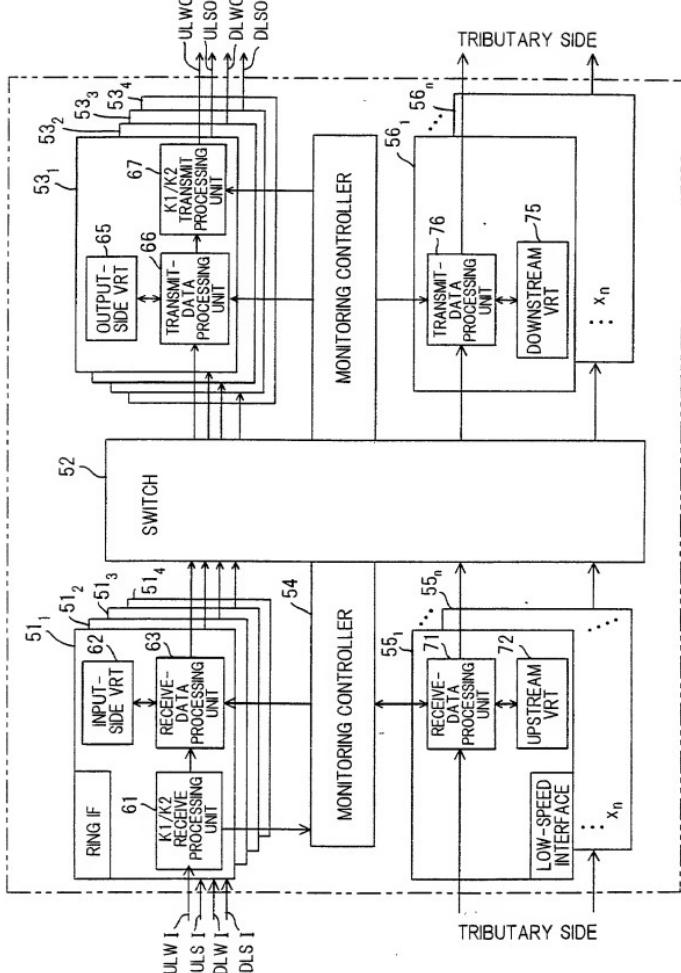


FIG. 2A

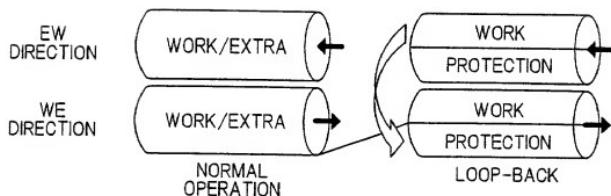
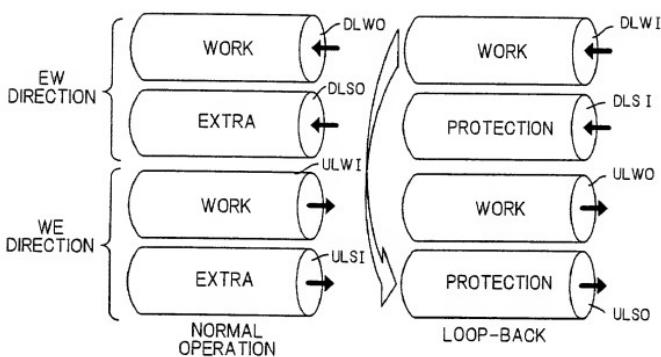


FIG. 2B



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FIG. 3

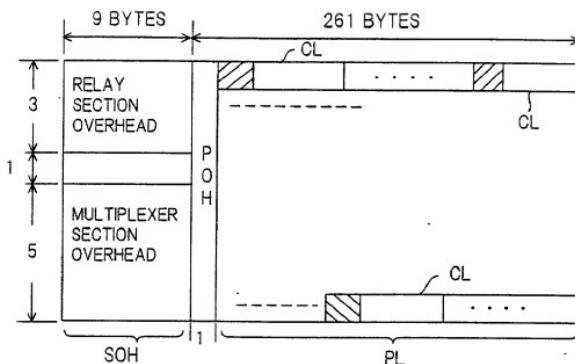


FIG. 4A

VPI/VCI	APPARATUS CID	ENABLE	ROUTING TAG (OUTPUT PORT)	-----
:	0	0		
:	1	1		
:	3	1		
:	4	1		-----
:	:	:		
:	:	:		
:	:	:		
:	65534	0		

FIG. 4B

APPARATUS CID	VRT
0	
1	
3	
4	-----
:	VPI, VCI
65534	(IP, Adr)

FIG. 5

VPI/VCI	APPARATUS CID	ENABLE	ROUTING TAG (OUTPUT PORT)	-----	SQUELCH TABLE
:	0	0			
:	1	1			
:	3	1			
:	4	1			
:	:	:			
:	:	:			
:	:	:			
:	65534	0			

FIG. 6

APPARATUS CID	VRT
0	
1	
3	
4	
:	
:	
:	
65534	<p style="text-align: center;">-----</p> <p style="text-align: center;">VPI, VCI (IP Addr)</p> <p style="text-align: center;">-----</p> <p style="text-align: center;"> </p> <p style="text-align: center;"> </p>

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FIG. 7

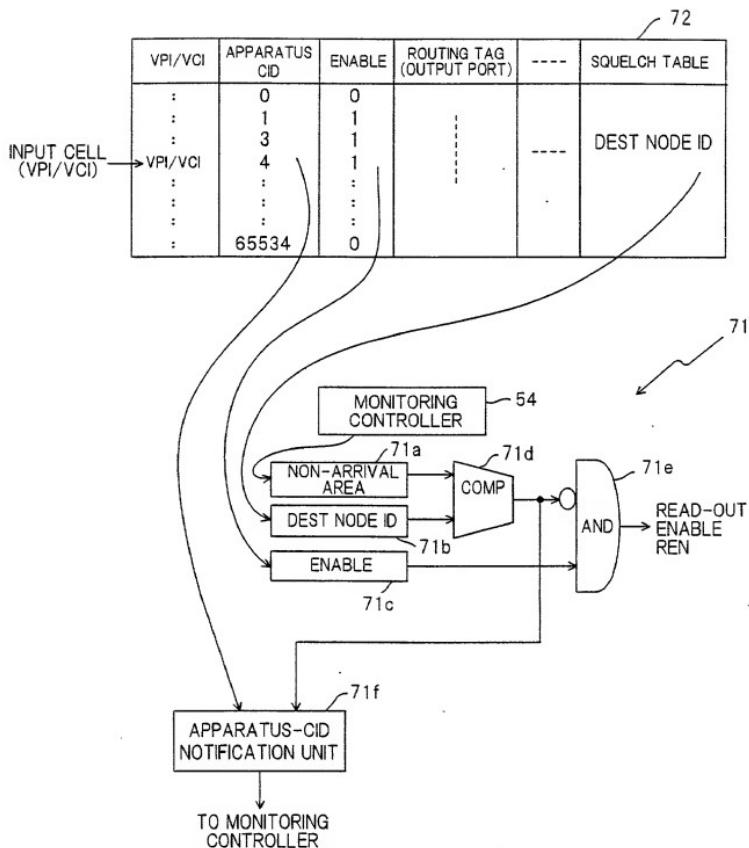


FIG. 8

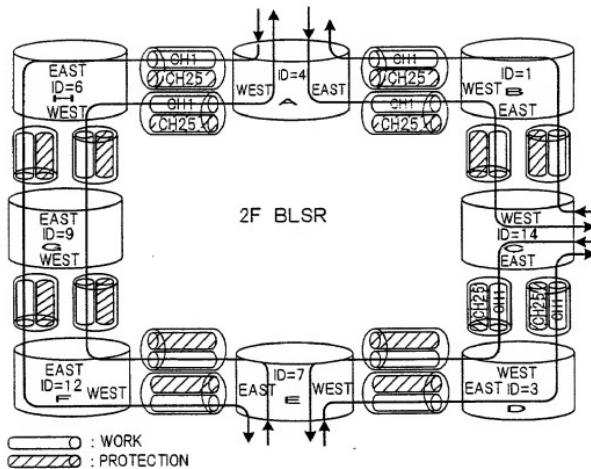


FIG. 9

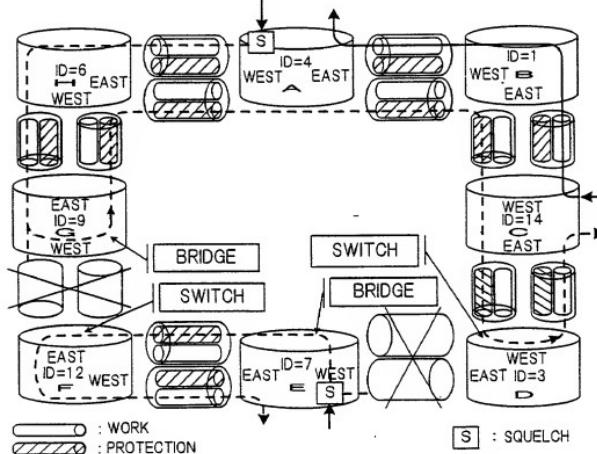
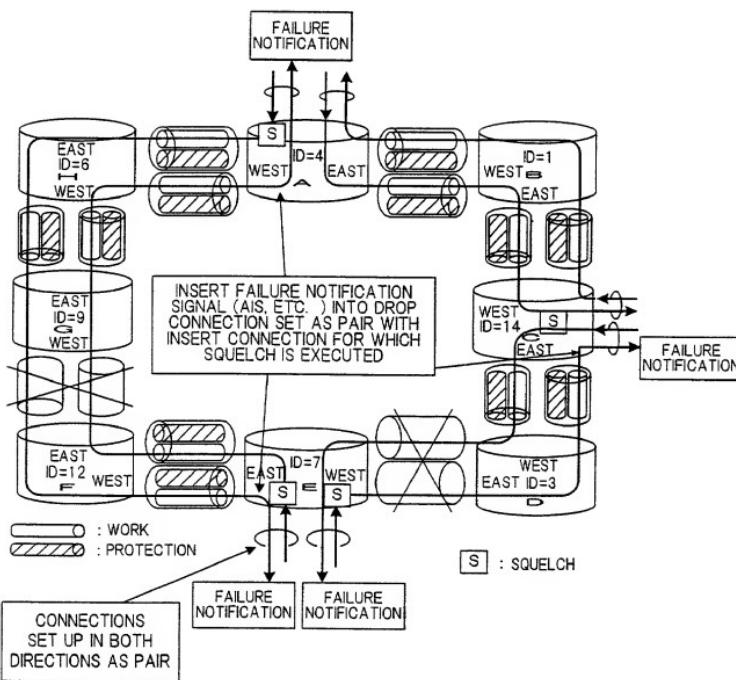
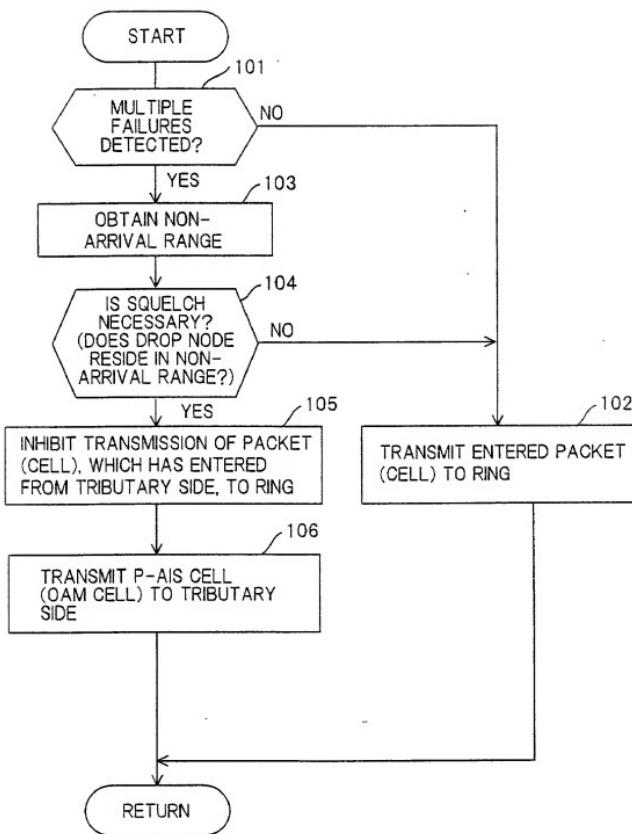


FIG. 10



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FIG. 11



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FIG. 12A

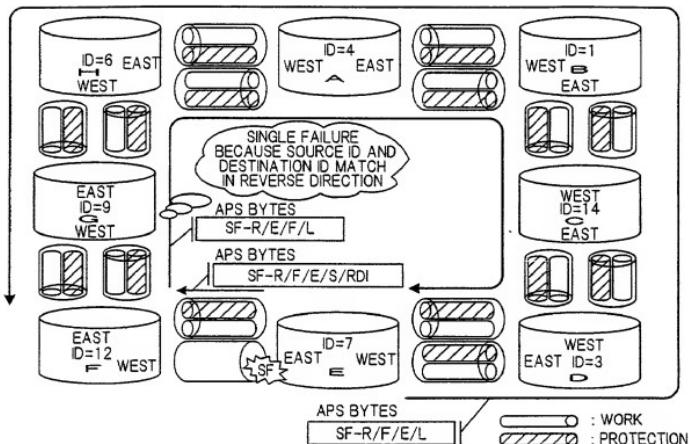


FIG. 12B

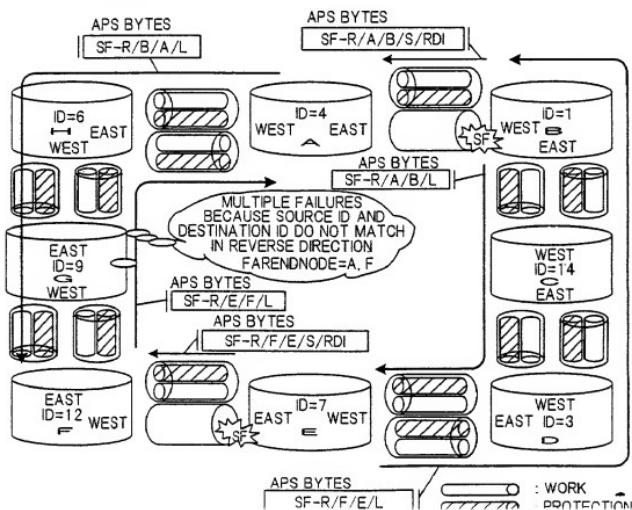


FIG. 13

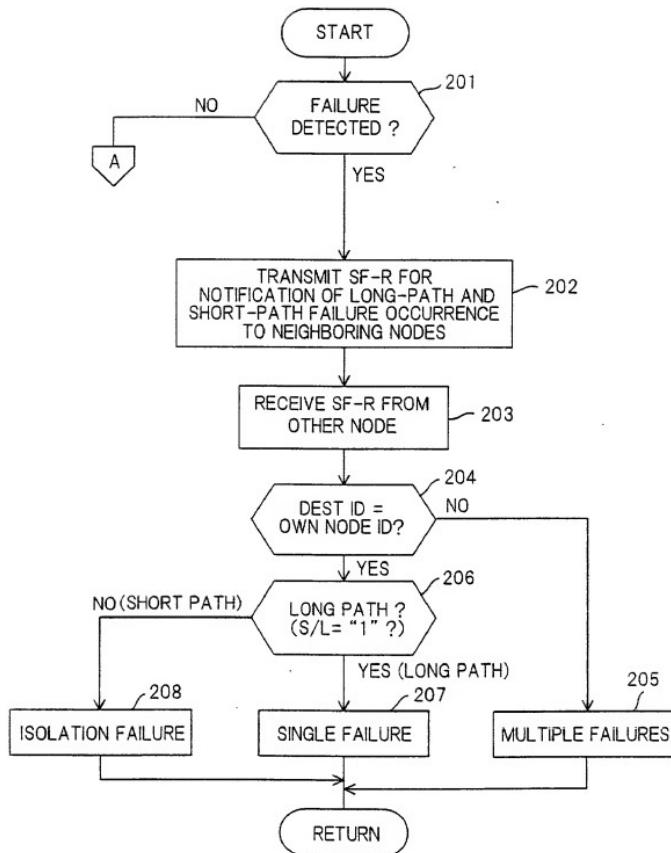
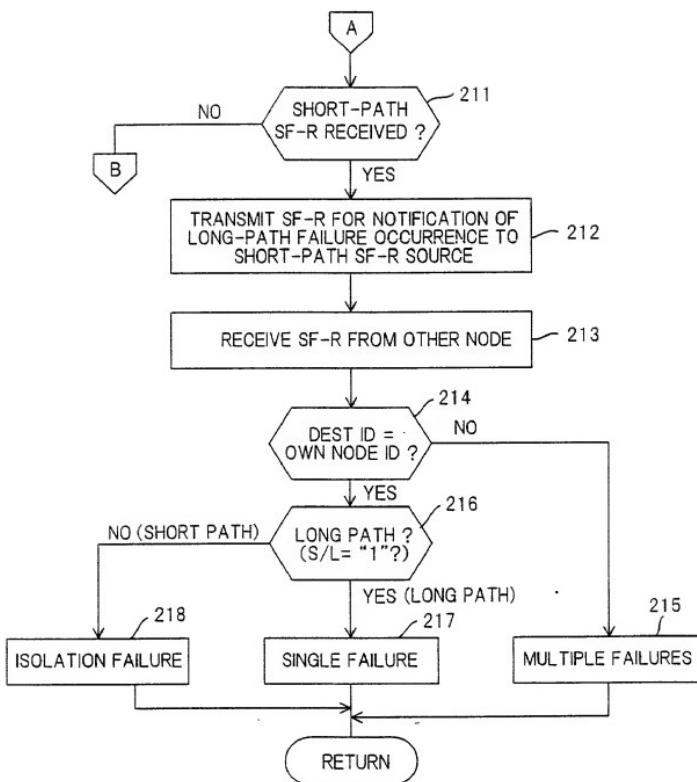


FIG. 14



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FIG. 15

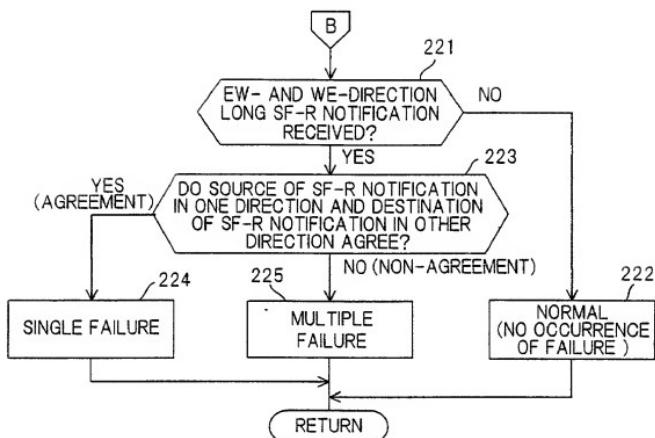


FIG. 16

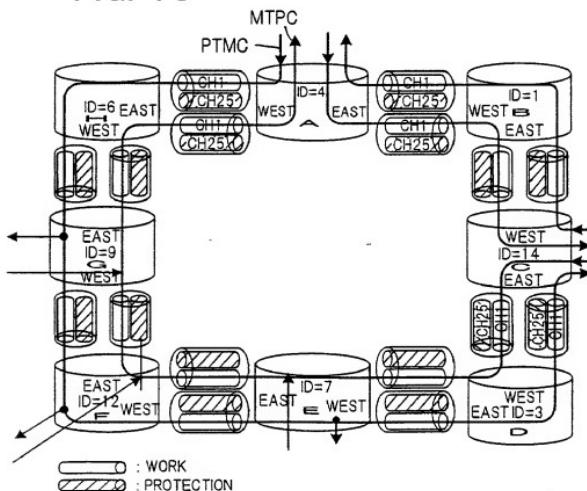


FIG. 17

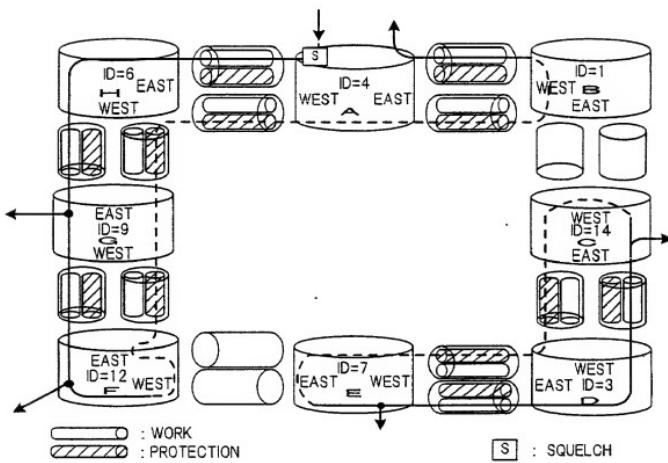


FIG. 18

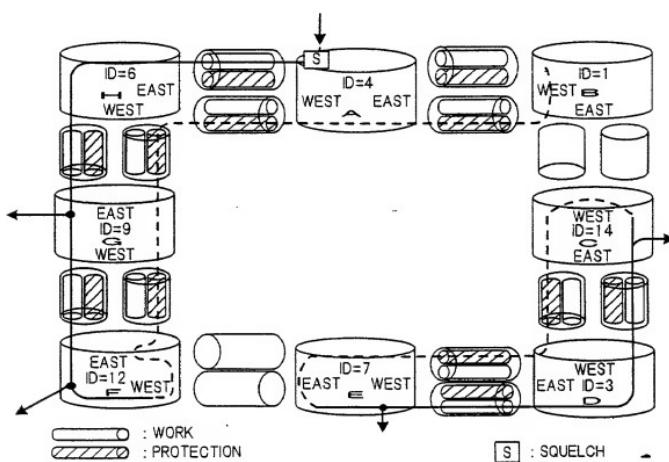
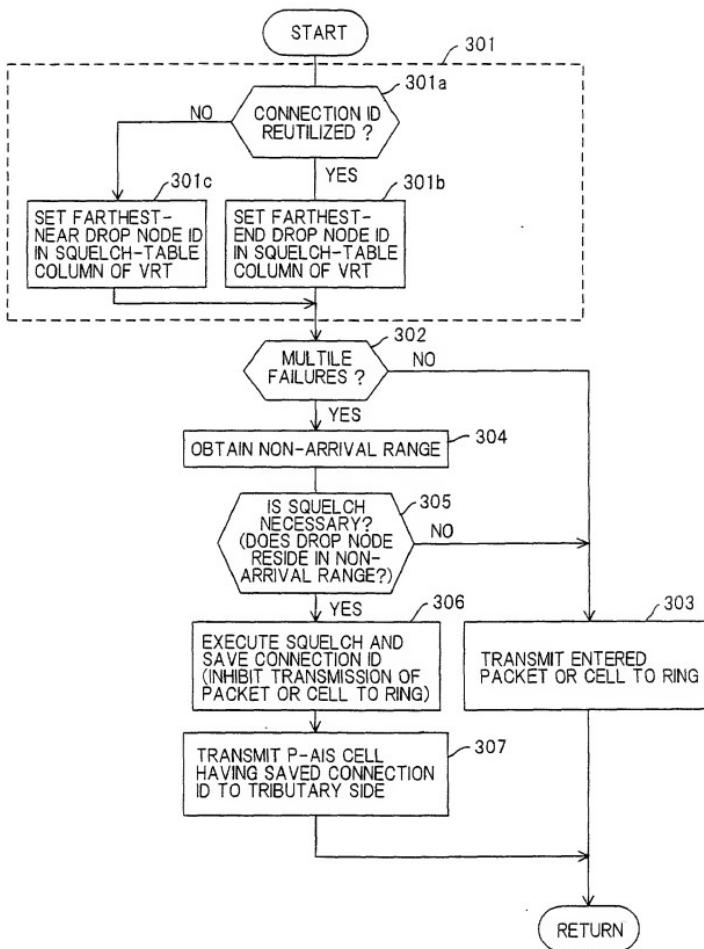


FIG. 19



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FIG. 20

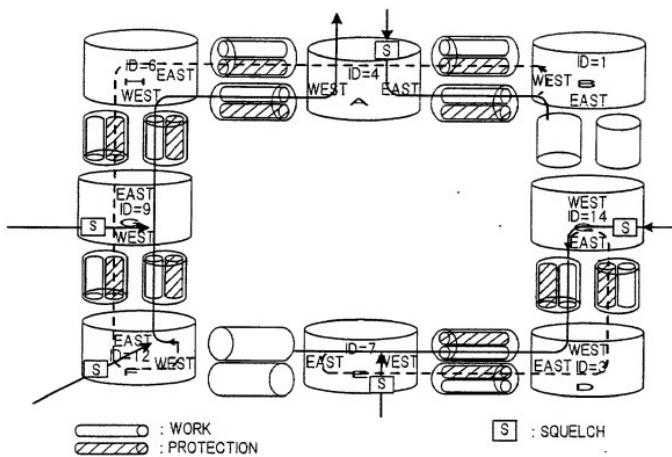
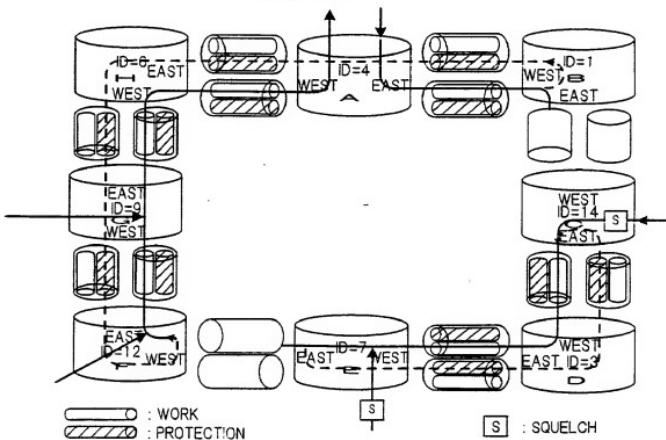
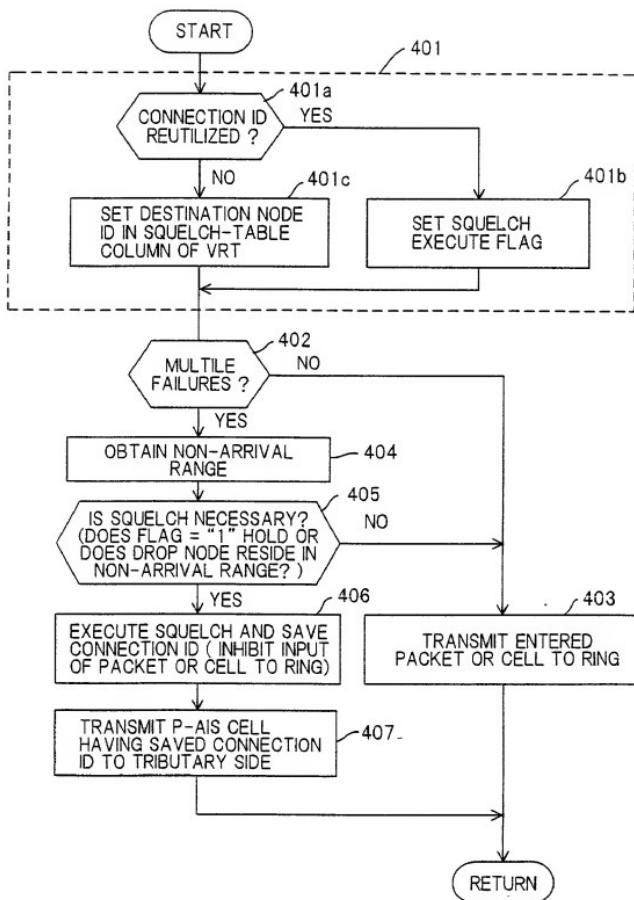


FIG. 21

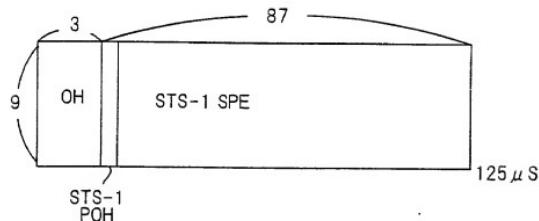
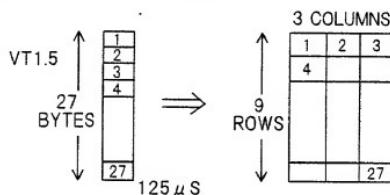


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FIG. 22



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FIG. 23A PRIOR ART*FIG. 23B PRIOR ART**FIG. 23C PRIOR ART*

→ STS-1 SPE COLUMNS

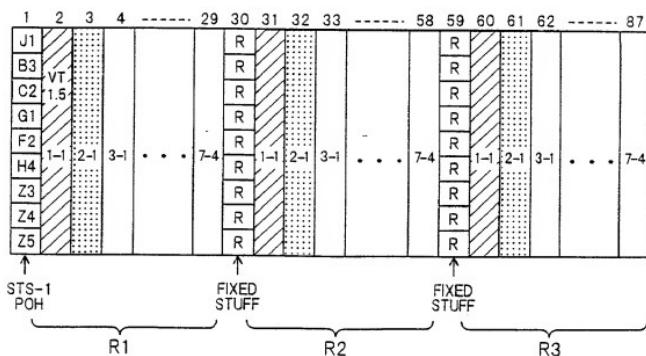


FIG. 24

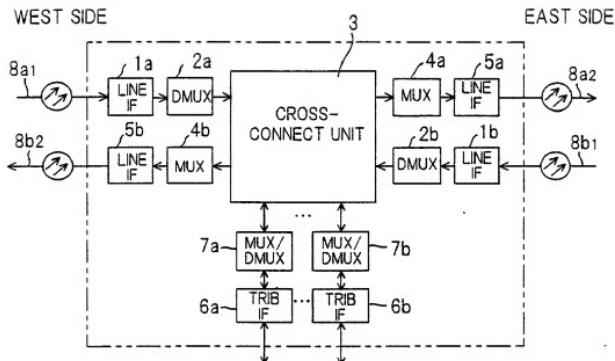


FIG. 25

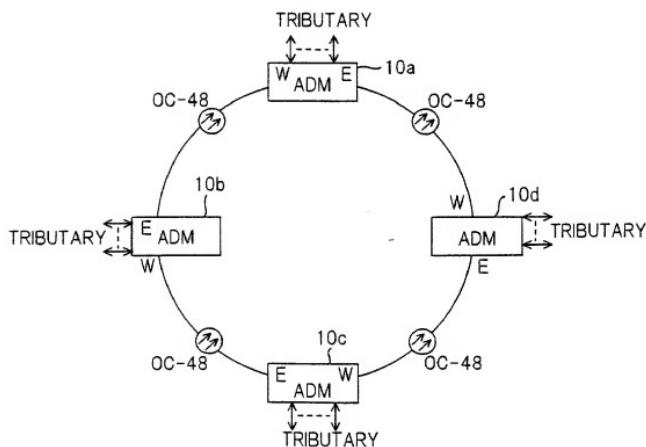
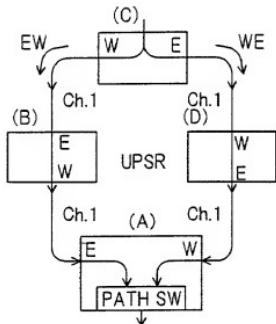


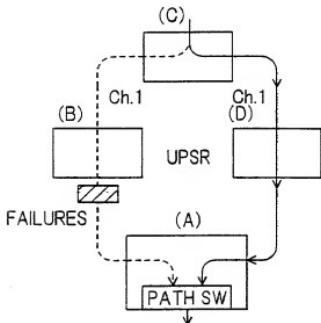
FIG. 26A PRIOR ART FIG. 26C PRIOR ART



The diagram illustrates the signal flow in the BLSR system. It features three main horizontal blocks labeled Ch.1, Ch.2, and Ch.3. Ch.1 contains a central unit (C) with inputs EW and WE, and outputs Ch.1 (B) and Ch.1 (D). Ch.2 contains a central unit (A) with inputs Ch.1 (B) and Ch.1 (D), and outputs Ch.2 (B) and Ch.2 (D). Ch.3 contains a central unit (E) with inputs Ch.2 (B) and Ch.2 (D), and outputs Ch.3 (B) and Ch.3 (D). The connections are as follows: EW connects to Ch.1 (B); Ch.1 (B) connects to Ch.2 (B); Ch.1 (D) connects to Ch.2 (D); Ch.2 (B) connects to Ch.3 (B); Ch.2 (D) connects to Ch.3 (D); and Ch.3 (B) and Ch.3 (D) both connect back to Ch.1 (B).

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FIG. 26B PRIOR ART FIG. 26D PRIOR ART



The diagram illustrates a complex control system architecture. At the top, a box labeled '(C)' is connected to a central junction point. From this junction, two parallel paths descend. The left path contains a box labeled 'Ch.1 (B)'. The right path contains a box labeled 'Ch.25'. These two paths converge at another junction point. From this junction, two more parallel paths descend. The left path contains a box labeled 'Ch.25 (D)'. The right path contains a box labeled 'Ch.1'. These final two paths converge at a bottom junction point. From this junction, two paths lead to boxes labeled '(A) Ch.25' and 'Ch.1'. A dashed line labeled 'FAILURES' originates from the junction point before the '(A) Ch.25' box and points towards the left side of the diagram. A hatched rectangle is located near the bottom left. The label 'BLSR' is positioned centrally below the main junction point.

FIG. 27 PRIOR ART

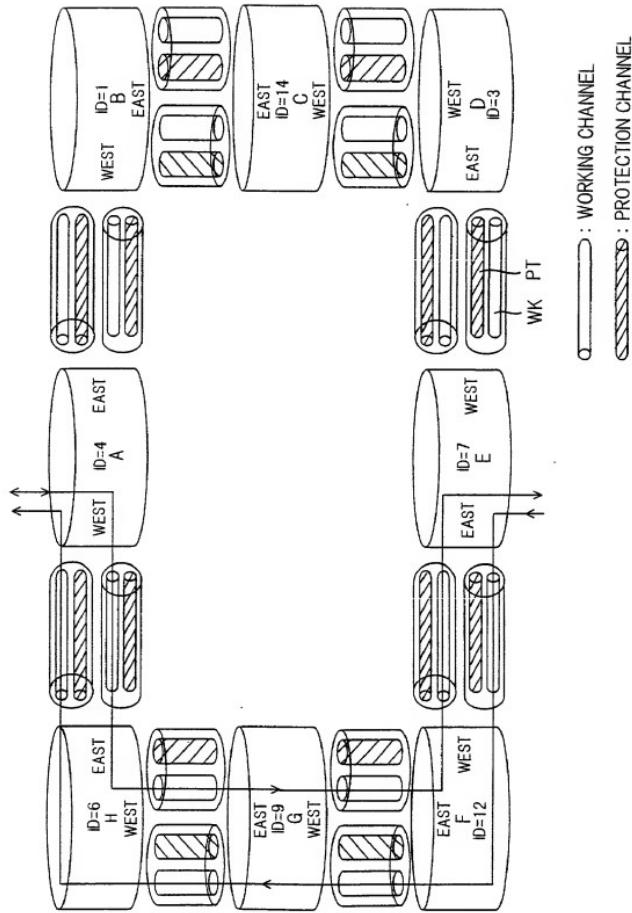


FIG. 28 PRIOR ART

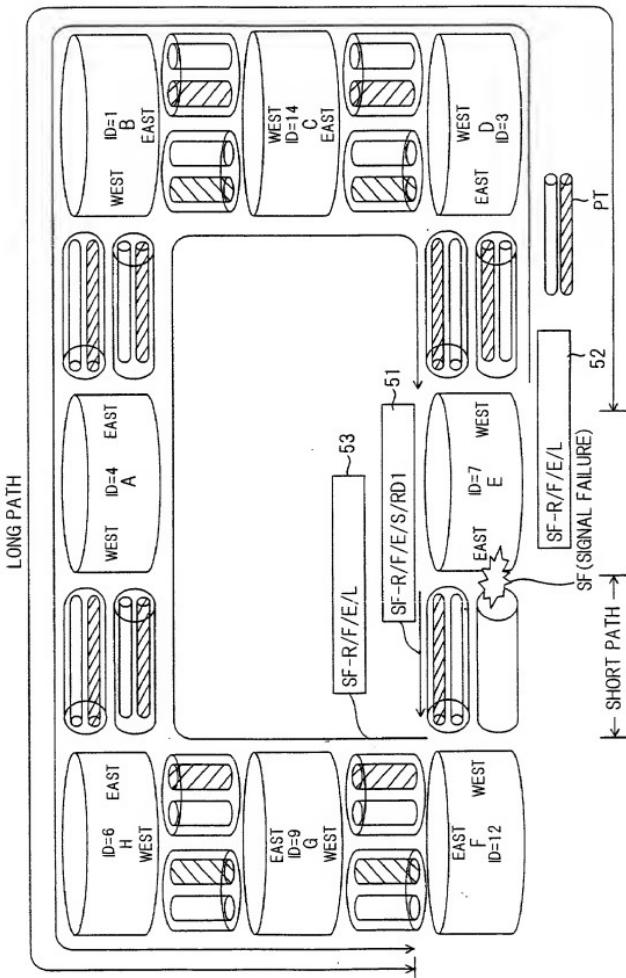


FIG. 29 PRIOR ART

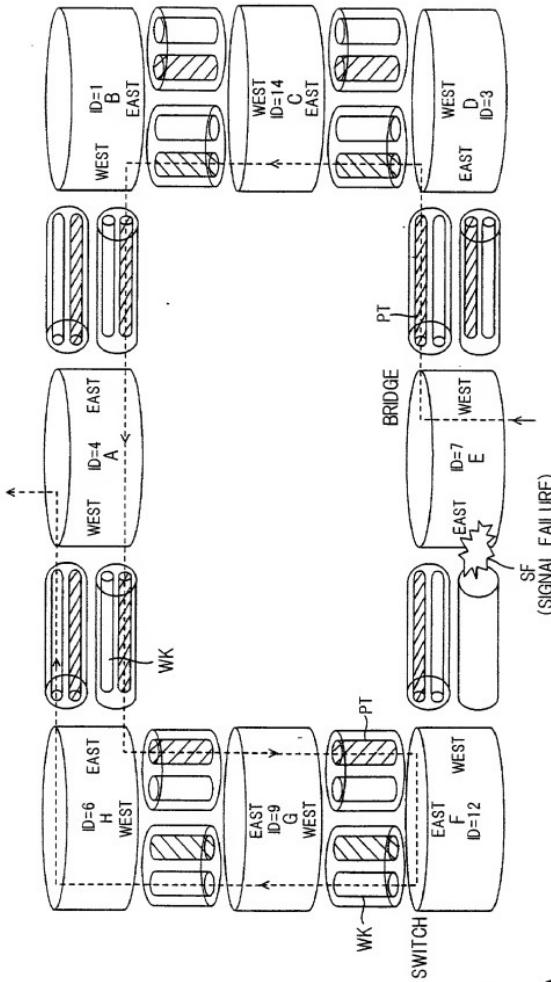


FIG. 30 PRIOR ART

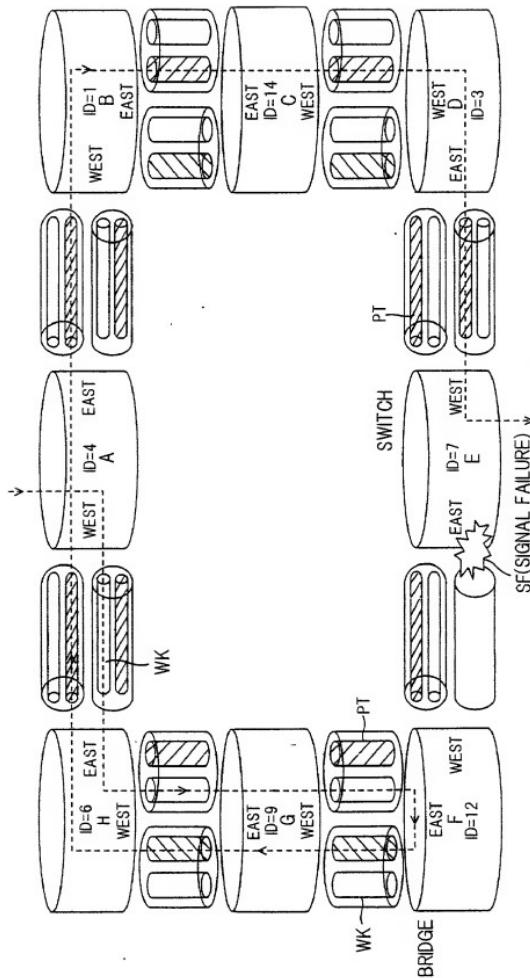


FIG. 31 PRIOR ART

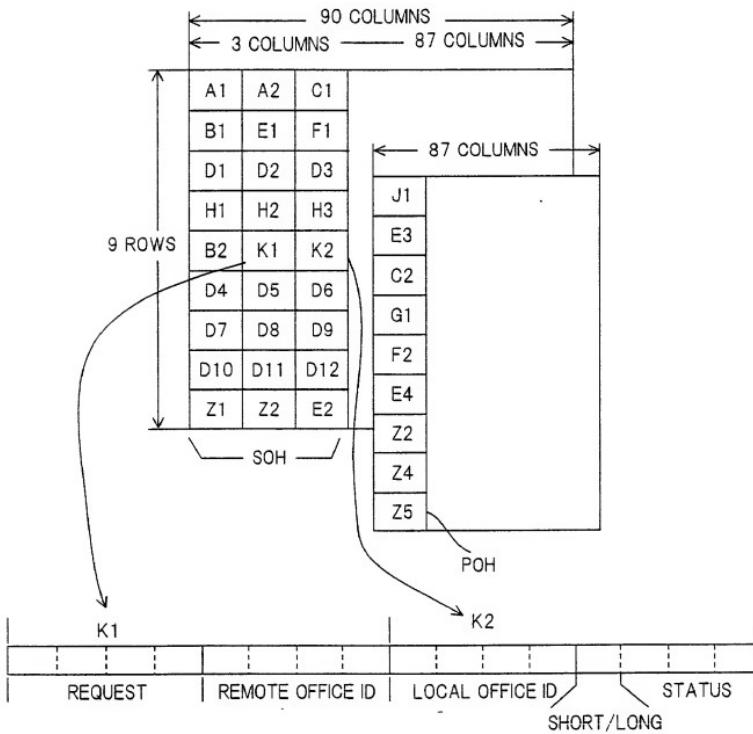
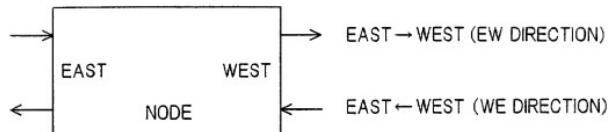


FIG. 32A PRIOR ART*FIG. 32B PRIOR ART*

SQUELCH TABLE

Ch1 (CN1)	WEST SIDE		EAT SIDE		DIRECTION
	SOURCE	DESTINATION	SOURCE	DESTINATION	
	DESTINATION	SOURCE	DESTINATION	SOURCE	
{	{	{	{	{	{
Ch. n

FIG. 33 PRIOR ART

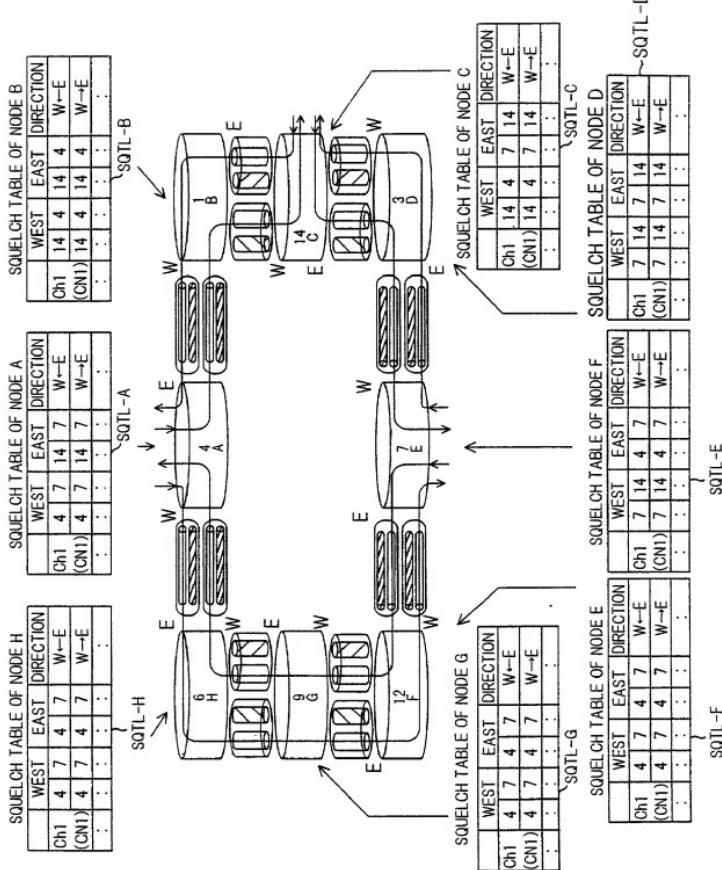
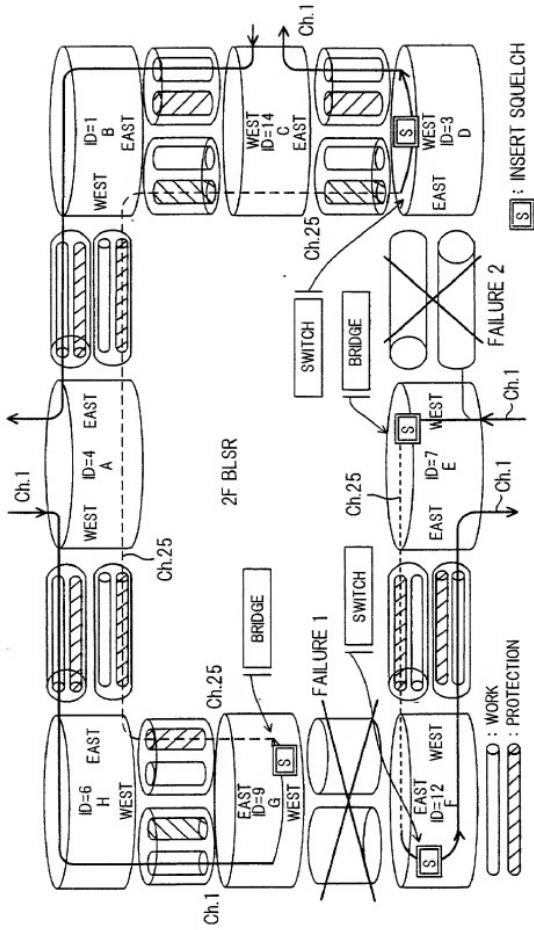


FIG. 34 PRIOR ART



SQUELCH TABLE OF NODE E																
INDEX	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
7	12	9	6	4	1	14	3	-	-	-	-	-	-	-	-	
(C1)	7	14	7	14	7	14	4	4	7	W-E						
:	:	:	:	:	:	:	:	:	:							

FIG. 35A PRIOR ART

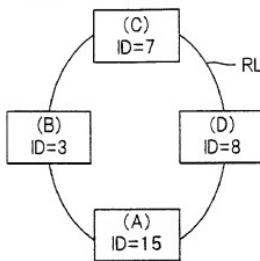


FIG. 35B PRIOR ART

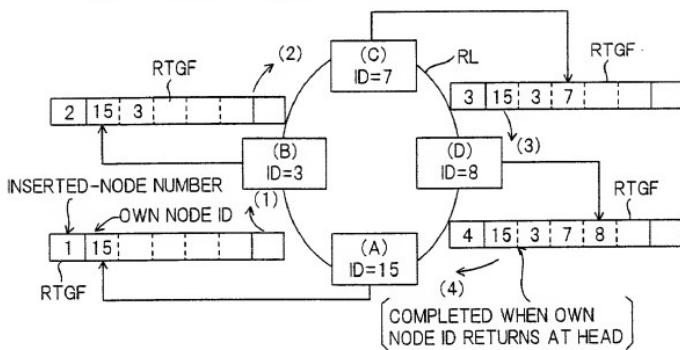


FIG. 35C PRIOR ART

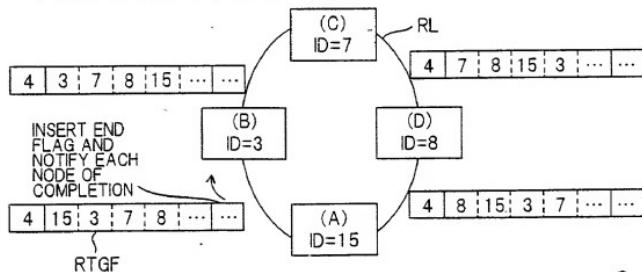


FIG. 36A PRIOR ART

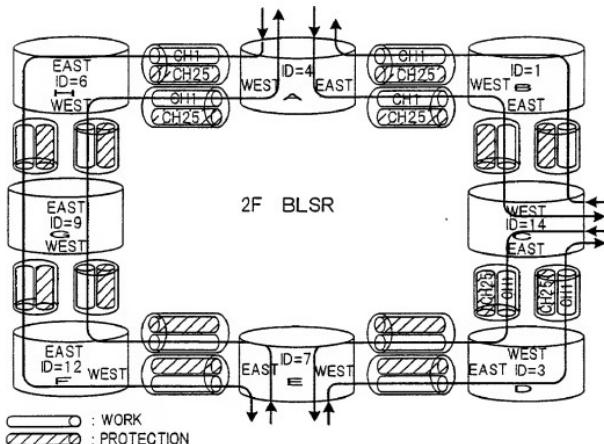


FIG. 36B PRIOR ART

